We Claim:

1. A dynamic random access memory (DRAM) having a shared sense amplifier organization concept, comprising:

sense amplifiers disposed in sense amplifier strips;

cell arrays subdivided into cell blocks having memory cells and bit lines connected as bit line pairs from two adjacent said cell blocks in each case to a common sense amplifier of said sense amplifiers, said sense amplifiers being disposed between said cell blocks, said bit lines having first ends and second ends connected to said sense amplifiers; and

bit line switches disposed in said sense amplifier strips, disposed between said cell blocks, between in each case two adjacent said sense amplifiers, said bit line switches momentarily connecting said first ends, not connected to said sense amplifiers, of two of said bit line pairs from adjacent said cell blocks during a precharge phase of a bit line pair activated directly beforehand, the precharge phase taking place at a start of a charge equalization phase.

2. The DRAM according to claim 1, further comprising a multiplicity of word lines running in said cell blocks of said cell arrays, said word lines intersecting said bit lines

substantially perpendicularly and activating said memory cells of said cell blocks.

3. The DRAM according to claim 1, further comprising charge equalization units each connected to one of said bit line pairs in said sense amplifier strips on a right and on a left of each of said sense amplifiers to short-circuit two bit line halves of each of said bit line pairs directly after an activation of a respective cell block to which a respective bit line pair belongs, for a charge equalization of said two bit line halves that are spread during an active phase of said respective cell block.

4. The DRAM according to claim 1, wherein to close each of said bit line switches, each of said bit line switches receives a control signal generated by a logical combination of charge equalization states of this and at least an adjacent cell block.

5. A method for operating a dynamic random access memory having a shared sense amplifier organization concept, the memory having cell arrays subdivided into cell blocks and bit lines connected in as bit line pairs to and extending from two adjacent cell blocks in each case to a common sense amplifier, and sense amplifiers being disposed between the cell blocks, which comprises the steps of:

momentarily interconnecting previously non-connected first ends of the bit line pairs connected to the sense amplifiers lying in two adjacent sense amplifier strips during a precharge phase for a relevant bit line pair, the precharge phase taking place at a start of a charge equalization phase, resulting in a precharge time for the relevant bit line pair being shortened.

6. The method according to claim 5, which further comprises activating the momentary interconnection of the two adjacent bit line pairs by a control signal generated by a logical combination of charge equalization states of the relevant cell block and of an adjacent cell block at a beginning of the charge equalization phase of the relevant cell block and the control signal is fed to a bit line switch pair disposed between the two bit line pairs to be connected.